WHAT IS CLAIMED IS:

1. A method for compressing a semiconductor integrated circuit, comprising:

dividing a design region, in which a semiconductor integrated circuit is to be designed, into a plurality of blocks;

assigning semiconductor devices to each of the blocks;

determining a device density of each block;

compressing any block that is determined to have a low device density; and

connecting the blocks by wiring.

2. The method for compressing a semiconductor integrated circuit according to claim 1, wherein the assigning of the semiconductor devices comprises:

assigning functions to the respective blocks by functional descriptions; and

obtaining standard cells by synthesizing the functional descriptions.

3. The method for compressing a semiconductor integrated circuit according to claim 1, wherein the assigning of the semiconductor devices comprises:

assigning standard cells, which are obtained by synthesizing functional descriptions, to each of the blocks.

4. The method for compressing a semiconductor integrated circuit according to claim 1, wherein in the

assigning of the semiconductor devices to each of the blocks, arrangement of the semiconductor devices is optimized on a block-by-block basis.

5. The method for compressing a semiconductor integrated circuit according to claim 1, wherein in the assigning of the semiconductor devices to each of the blocks, the semiconductor devices assigned to at least one of the blocks are designed by a custom layout, and the semiconductor devices assigned to the other blocks are designed by standard cells.

6. The method for compressing a semiconductor integrated circuit according to claim 5, wherein in the assigning of the semiconductor devices to each of the blocks, the semiconductor devices assigned to a plurality of the blocks are designed by a custom layout, and the semiconductor devices assigned to the other blocks are designed by standard cells, and

a mutual positional relationship between the plurality of the blocks, to which the semiconductor devices are assigned by the custom layout, is kept unchanged at a time of optimization.

7. The method for compressing a semiconductor integrated circuit according to claim 1, wherein the size of each of the divided blocks is set such that when the positions of the semiconductor devices are shifted within the block, a wiring delay due to the shift does not affect an operation of the semiconductor

integrated circuit.

8. The method for compressing a semiconductor integrated circuit according to claim 7, wherein a time of the wiring delay, which varies when the positions of the semiconductor devices are shifted within each block, is 1% or less of an operational clock cycle of the semiconductor integrated circuit.

9. The method for compressing a semiconductor integrated circuit according to claim 1, wherein the compressing of the block includes overlapping adjacent blocks with the low device density and overlapping a block with the low device density and a block with a high device density, which are located adjacent to each other.

10. The method for compressing a semiconductor integrated circuit according to claim 1, wherein the compressing of the block includes reducing the size of a block with a low device density.

11. The method for compressing a semiconductor integrated circuit according to claim 1, further comprising:

determining a wiring density in the block, which is determined to have the low device density, prior to the compressing of the block; and

determining any block found to have a wiring density equal to or higher than a predetermined value, to be one that has a high device density.

12. The method for compressing a semiconductor integrated circuit according to claim 1, further comprising:

determining, prior to the compressing of the block, whether the blocks, which are determined to be "dense", concentrate in a specific row or column; and

reducing, when the block, which have the high device density, are determined to concentrate in a specific row, the horizontal dimension of each block, which has the high device density, without varying the area of the block, and reducing, when the blocks, which have the high device density, are determined to concentrate in a specific column, the vertical dimension of each block, which has the high device density, without varying the area of the block.

13. The method for compressing a semiconductor integrated circuit according to claim 1, wherein a compression ratio of the block is determined in accordance with a required shape of an entire design.

14. The method for compressing a semiconductor integrated circuit according to claim 13, wherein an aspect ratio of the block is changed in accordance with a required shape of an entire design.

15. A method for compressing a semiconductor integrated circuit, comprising:

dividing a design region, in which a semiconductor integrated circuit is designed and semiconductor

devices are assigned, into a plurality of blocks;

determining a device density of each block;

compressing any block that is determined to have a low device density; and

connecting the blocks by wiring.

16. The method for compressing a semiconductor integrated circuit according to claim 15, wherein the size of each of the divided blocks is set such that when the positions of the semiconductor devices are shifted within the block, a wiring delay due to the shift does not affect an operation of the semiconductor integrated circuit.

17. The method for compressing a semiconductor integrated circuit according to claim 16, wherein a time of the wiring delay, which varies when the positions of the semiconductor devices are shifted within each block, is 1% or less of an operational clock cycle of the semiconductor integrated circuit.

18. The method for compressing a semiconductor integrated circuit according to claim 15, wherein the compressing of the block includes overlapping adjacent blocks with the low device density and overlapping a block with the low device density and a block with a high device density, which are located adjacent to each other.

19. The method for compressing a semiconductor integrated circuit according to claim 15, wherein

the compressing of the block includes reducing the size of a block with the low device density.

20. The method for compressing a semiconductor integrated circuit according to claim 15, further comprising:

determining a wiring density in the block, which is determined to have the low device density, prior to the compressing of the block; and

determining any block found to have a wiring density equal to or higher than a predetermined value, to be one that has a high device density.

21. The method for compressing a semiconductor integrated circuit according to claim 15, further comprising:

determining, prior to the compressing of the block, whether the blocks, which are determined to be "dense", concentrate in a specific row or column; and

reducing, when the blocks, which have the high device density, are determined to concentrate in a specific row, the horizontal dimension of each block, which has the high device density, without varying the area of the block, and reducing, when the blocks, which have the high device density, are determined to concentrate in a specific column, the vertical dimension of each block, which has the high device density, without varying the area of the block.

22. The method for compressing a semiconductor

integrated circuit according to claim 15, wherein a compression ratio of the block is determined in accordance with a required shape of an entire design.

23. The method for compressing a semiconductor integrated circuit according to claim 22, wherein an aspect ratio of the block is changed in accordance with a required shape of an entire design.